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Methodology for Verifying Multi-Cycle and Clock-Domain-Crossing Logic Using Random Flip-Flop Delays

Abstract

A design tool inserts randomized delays into synchronizers for signals crossing from one clock domain to another. Rather than having a wide range of random delays to select from, each synchronizer's randomized delay is selected from only two possibilities. An added delay of either zero or one clock period of the new domain's clock is added as the randomized delay. The randomized delay causes the re-synchronized domain-crossing signal to become available either in the expected cycle or in the cycle following the expected cycle. Logic hazards caused by the domain-crossing signal can be detected and the possible results simulated. The synchronizer can be a series of two flip-flops, with the random delay added to the first flip-flop. Randomized delays of either one or none added periods of the clock can also be added to multi-cycle signals within one clock domain that have two or more clock cycles to propagate.